Analytical electro-thermal model and 3-D thermal resistance network for SMD-based printed circuit board power converters

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***Abstract*—This work presents an analytical electro-thermal model for SMD-based printed circuit board (PCB) power converters. Temperature-dependent component losses are derived from analytical models and a 3-D thermal resistance network is employed to characterize the temperatures across components and PCB paths. Furthermore, the work explores the mechanical and thermal interaction within the PCB paths, concurrently analyzing semiconductor switches and the power inductor in synchronous commutation cell configurations. The proposed model undergoes evaluation with two different PCB layouts of a synchronous boost converter, operating at 350 kHz with 50 W and 75 W. Model-generated temperatures are compared with experimental measurements using a thermal imaging camera and with Finite Elements Analysis (FEA) in Ansys Icepak. The acquired results validate the accuracy of the proposed model.**

***Index Terms*—Finite Elements Analysis, PCB layout, Power electronics, Synchronous commutation cell, Thermal modeling.**

I. Introduction

In the last decade, many efforts have been directed at power electronics to make power converters more efficient, compact, reliable, and low-cost [1]–[4]. Among different techniques, the efficiency and power density maximization of the converter can be accomplished by wide bandgap (WBG) semiconductor technologies [5]–[7]; switching frequency rising; printed circuit board (PCB) layout parasitic minimization [8]–[10] and thermal management [11], [12].

Advancements in surface mount device (SMD) technology have significantly enhanced the performance and efficiency of power semiconductors, reducing parasitic inductances and making them suitable for various applications, from consumer electronics to industrial equipment [13]. SMD power MOSFETs are soldered directly onto the PCB surface, significantly reducing occupied space. However, due to their smaller exposed surfaces, their heat dissipation capabilities may be limited compared to through-hole MOSFETs, and adequate thermal management of the PCB is necessary to ensure efficient heat dissipation [14], [15].

Power converter topologies including buck, boost, and buck-boost, employ low-side and high-side half-bridge configurations with a power inductor, forming a synchronous commutation cell [16]–[18]. Traditionally, thermal management in a synchronous commutation cell is achieved using PCB paths and heat sinks or coolers, which dissipate heat from semiconductors to the environment, thereby reducing junction-ambient thermal resistance [19]–[21]. Nevertheless, a recent approach reveals the potential to transfer heat from SMD hot spots to the ambient environment solely through PCB paths and thermal vias, obviating the need for additional heat sinks or coolers [22].

Research that analyzes the PCB mechanical characteristics and the thermal behavior of semiconductor switches and power inductors is presented in different works in the literature. In [22], an algorithm is developed to optimize the mechanical characteristics of pads, such as PCB path length, and width to minimize the thermal resistance and maximize the heat flow rate from SMD semiconductors.

An electro-thermal design methodology for a synchronous buck converter is discussed in [23] and [24]. The PCB layout is developed with internal layers of PCB paths that maximize the heat transfer from the semiconductors to the ambient, minimizing its junction temperatures.

A design and thermal characterization of a high power density SMD GaN-based synchronous buck converter is proposed in [25]. The authors have considered the thermal coupling among the semiconductor switches and the power inductor. This also presents a simplified 2-D thermal resistance model to estimate the semiconductor junction temperature and the inductor temperature. An analytical method to estimate the PCB paths, case, and junction temperature of semiconductor switches is discussed in [26]. This method is based on Fourier series and finite volume techniques, with the main objective being to describe the thermal estimation of the PCB elements considering radiation heat transfer between the PCB and the ambient.

In [27], the authors proposed an analytical method based on

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finite differences to estimate transient and steady-state junction temperatures in IGBTs attached to a power module. Moreover, through a ZVS full-bridge with a magnetic coupling power converter, the transient and steady-state temperatures of IGBTs are compared and validated through experimental results.

A method of thermal estimation for two IGBTs and two diodes attached to a power module is presented in [28]. The method makes use of an electrical circuits simulator and Finite Element Analysis (FEA) simulation to determine a thermal interaction that occurs among the components and their thermal behavior. The electrical simulator estimated the power losses in the IGBTs and the diodes, and the FEA evaluated separately the thermal interaction among them. The authors created an equivalent thermal capacitance and resistance matrix that relates the losses of the elements, their junction temperature, and the temperature of the heat sink of the power module.

In addition, [29] discusses a study focused on estimating losses and determining the optimal thermal placement of power electronic modules. The loss estimation is performed by analytical models. The paper employs the FEA method for solving conductive heat transfer in the complex geometry of a three-phase inverter, integrating it with a genetic algorithm (GA) to optimize thermal chip placement. This method significantly reduced FEA efforts.

From methodologies employed in the literature, it is noted that works [23] and [24] lack an analysis of PCB paths and their impact on the junction temperature of semiconductors. [25] necessitates the implementation of a physical prototype, while [26] involves complex methods that are challenging to implement. Furthermore, [27] does not address the thermal behavior in PCBs with thermal vias, and [28] and [29] require FEA to extract thermal impedance among the elements. However, the use of FEA presents challenges, given its licenses, computational processing time, and significant human resources involved in the simulation [30], [31].

Based on these considerations, this paper proposes an analytical electro-thermal model for an SMD-based synchronous commutation cell. The model uses temperature-dependent electrical losses obtained through analytical models and a 3-D thermal resistance network, enhancing the accuracy of thermal estimation, and providing precise, and reliable results without the need for FEA simulation or the prototyping process.

The paper additionally assesses the mechanical and thermal interaction within the PCB paths, simultaneously analyzing the semiconductor switches in both low-side and high-side half-bridge configurations, along with the power inductor. This analysis empowers the PCB designer to evaluate the impact of each component on converter power losses and their contribution to the thermal behavior of the synchronous commutation cell.

To systematically present the findings, the work is structured as follows. Section II outlines and models the three heat transfer mechanisms from PCB to ambient. Subsequently, Section III employs these mechanisms for the thermal modeling and characterization of the SMD-based synchronous commutation cell. This is performed by the development of an analytical electro-thermal model and a 3-D thermal resistance network. Section IV provides a description of the FEA and experimental setup. The experimental results are discussed in Section V. Section VI concludes the work.

II. Heat transfer in PCBs

The three basic heat transfer mechanisms from PCB to ambient are conduction, convection, and radiation. An equivalent electrical circuit can accomplish the heat transfer mechanism, in which the conduction, convection, and radiation are expressed as thermal resistances. Thus, the next sections present the thermal resistance equations in Sections II-A, II-B, and II-C for conduction, convection, and radiation respectively. In Section II-D is presented the extended surface modeling and in Section II-E the application of these models in a PCB.

A. Conduction

Conduction heat transfer in a PCB occurs when a hot spot delivers energy to the PCB path as a result of adjacent high and low-energy particle exchange. Thus, in (1) it is shown an equivalent conduction thermal resistance which appears in the area between the hot spot and the PCB path extension. Moreover, in (2) it is presented a conduction heat transfer thermal resistance inside the PCB, through the FR4 epoxy dielectric material [12], [32], [33].

$$R_{\theta cond} = \frac{l}{k_{Cu}.t_{Cu}.w} \tag{1}$$

where l represents the length between the hot spot and the PCB path end, k_{Cu} the copper thermal conductance, t_{Cu} the PCB copper plane thickness, and w the PCB path width.

$$R_{\theta PCB} = \frac{t_{PCB}}{k_{FR4}.A_{max}} \tag{2}$$

where k_{FR4} is the FR4 epoxy thermal conductance, t_{PCB} the PCB thickness and A_{max} the PCB maximum surface.

Thermal vias are also used in PCB layout to improve the heat transfer from a hot spot to the ambient. As presented in [22]. Thermal vias are holes made with a plating material, filled with air or a metallic element which connects two different PCB layers to provide an effective thermal path, and (3) defines the thermal resistance in accordance to the via diameter, plating thickness, and filler material properties [33].

$$R_{\theta via} = R_{\theta filler} // R_{\theta barrel} \tag{3}$$

where $R_{\theta filler}$ is defined in (4) and represents the thermal resistance of the filler material along a thermal via; and $R_{\theta barrel}$, calculated by (5), the thermal resistance of the plating material, attached to a PCB hole.

$$R_{\theta filler} = \frac{t}{k_{filler}.\pi(\frac{\phi}{2} - t_{pth})^2} \tag{4}$$

$$R_{\theta barrel} = \frac{t}{k_{Cu}.\pi.t_{pth}(\phi - t_{pth})} \tag{5}$$

where t_{pth} is the plating thickness, ϕ the via diameter, k_{filler} the thermal conductivity of the filler material and t, the PCB thickness. Also, when more than one thermal via is placed

near a heat source, its equivalent thermal resistance is equal to a parallel association of all thermal vias, given by (6).

$$R_{\theta via(equiv)} = \frac{R_{\theta via}}{n_{vias}} \tag{6}$$

where n_{vias} is the number of vias attached to a PCB path.

B. Convection

Convection heat transfer is a combination of conduction and fluid motion and can be classified as natural or forced. In natural convection, every fluid motion is caused by natural ways, such as hot fluid moving upward and cold fluid moving downward [12].

The thermal resistance that represents the convection heat transfer can be expressed as,

$$R_{\theta conv} = \frac{L_C}{k_{air}.Nu.A} \tag{7}$$

where L_C is the critical length, k_{air} is the air thermal conductance, Nu the Nusselt coefficient, and A the PCB path surface area [12], [32], [33].

When a PCB presents a horizontal positioning the L_C is defined as,

$$L_C = \frac{A}{p} \tag{8}$$

where p is the whole boundary of the PCB path or its perimeter.

Nusselt coefficient represents the relation between conduction and convection [32], which occurs inherently in the convection heat transfer process and is defined in,

$$Nu = \left[0.825 + \frac{0.387 + Ra^{\frac{1}{6}}}{\left[1 + \frac{0.492}{0.71}^{\frac{9}{16}}\right]^{\frac{8}{27}}}\right]^2 \tag{9}$$

where Ra is the Rayleigh coefficient which describes a relation between fluctuation and viscosity in a fluid, expressed as,

$$Ra = \frac{g\beta_{ar}\Delta T L_C^3 0.71}{\nu^2} \tag{10}$$

where g is the gravitational force of the Earth, β_{ar} the air thermal expansion coefficient, ΔT the maximum variation temperature, and ν the air viscosity.

C. Radiation

The thermal resistance which represents the radiation heat transfer process is expressed in (11), and it is inversely proportional to the material emissivity coefficient (ε), Steffen-Boltzmann constant (σ), the surface temperature (T_{top}) and the PCB path surface area (A), T_∞ represents the ambient temperature [32], [33],

$$R_{\theta rad} = \frac{1}{\varepsilon\sigma(T_{top} - T_\infty)^3 A}. \tag{11}$$

D. Extended Surfaces

Additionally, PCB paths can be modeled as extended surfaces or fins. It is considered that there is no heat generation, convective heat transfer (h_{conv}), and conductive heat transfer (k) remains constant along the fin [32], [33]. Also, supposing that the boundary does not transfer heat to the ambient, the thermal resistance that represents the fin is defined in 12. More details of constructive characteristics of fins are presented in [32], [33].

$$R_{\theta fin} = \frac{1}{\eta_a h_{conv} L w} \tag{12}$$

where η_a is the fin efficiency, explained in details by [33].

E. PCB Thermal Behavior

The components of an electronic circuit built in a PCB, are represented as current sources in the equivalent thermal circuit. These heat sources are connected in the system with equivalent thermal resistances in the x, y, and z directions (3-D), immersed in the ambient air (ambient temperature).

Thus, from the thermal resistance description, it is possible to note the influence of mechanical characteristics of PCB paths and the heat transfer rate from heat sources to ambient. Furthermore, to model the whole system accurately, it is necessary to build thermal resistance network. This can be used to evaluate the thermal coupling among the PCB paths and the heat sources to estimate the temperatures in the components. Figure 1 expresses an SMD-based component attached to a PCB with different thermal resistances, which are the opposition to heat transfer to ambient.

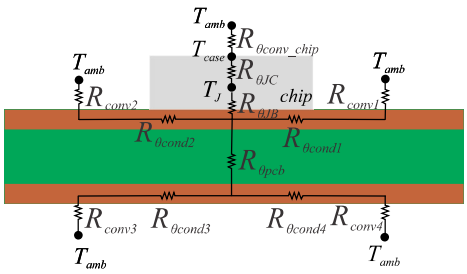
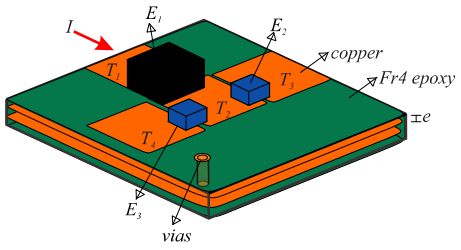


Fig. 1. SMD-based chip and the thermal resistances in a PCB.

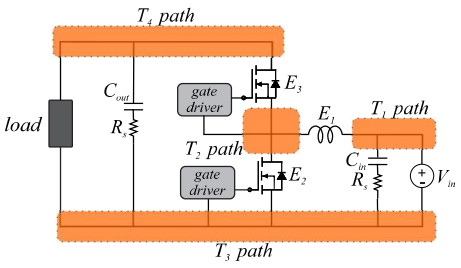
III. Thermal Modeling and Characterization of a Synchronous Commutation Cell

As aforementioned, in this work, a boost synchronous commutation cell is used as a case study. To demonstrate the PCB mechanical characteristics, Figure 2 (a) illustrates a commercial PCB with four conduction planes, a top layer making the PCB paths, two inner layers, and the bottom layer, separated by a dielectric material made of FR4 epoxy. Also, it presents the SMD inductor and the two SMD semiconductor switches. Its equivalent electrical circuit is shown in Figure 2 (b).

In these, E_1 is the power inductor, E_2 and E_3 are the low-side and high-side semiconductor switches, respectively.



(a)



(b)

Fig. 2. Synchronous boost converter. (a) Components distribution and its PCB paths. (b) Electrical circuit

T_1, T_2, T_3, and T_4 are the PCB paths among the electronic device, which connect the input voltage, the output voltage, and the power converter components. I is the electrical current, and e represents the spacing between conduction planes. Besides that, the DC-DC converter acts as a dimmable LED driver, where a closed-loop control system regulates the power transferred to the load.

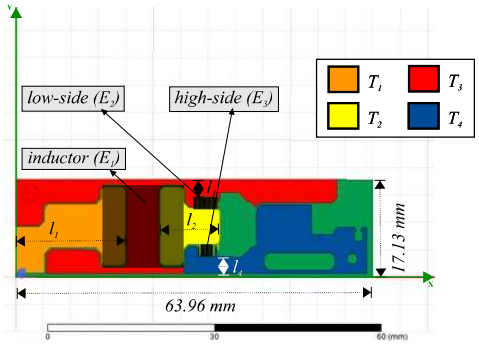
Considering a synchronous boost configuration, the input current will be applied in the T_1 path. The electrical current circulates through the inductor, to T_2, and arrives at T_3 when E_2 is on-state. When the E_2 is off-state, E_3 is on-state and the energy stored in the inductor is delivered to the load through T_4. The T_3 path is connected to the ground plane, and the T_4 path is the power converter output voltage terminal.

T_1, T_2, T_3, and T_4 PCB path mechanical characteristics influence actively the heat transfer process in the power converter. T_2 and T_3 modify E_2 behavior and its junction temperature (T_J), due to conduction and convection heat transfer to ambient. Also, E_2 transfers the heat to the ambient vertically through the PCB from top to bottom, and by convection through its package. Furthermore, T_2 and T_4 influences the E_3 semiconductor temperature.

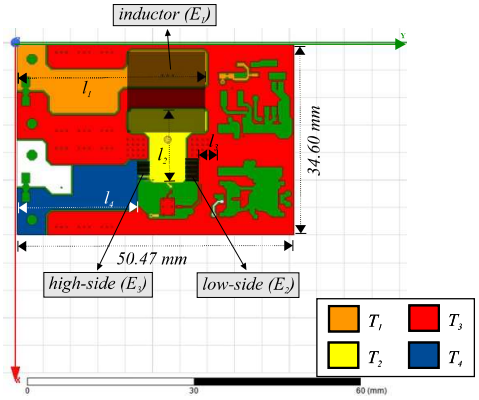
TABLE I
SYNCHRONOUS BOOST ELECTRICAL CHARACTERISTICS.

Variable	Symbol	Value
Input voltage	V_{in}	$12V$
Output voltage	V_{out}	$53.70V$
Nominal output power	P_{out}	$75\ W$
Switching frequency	f_{sw}	$350kHz$
Input capacitor	C_{in}	$10\mu F$
Output capacitor	C_{out}	$10\mu F$
Power inductor	E_1	$33\mu H$
High-side switch	E_3	$EPC\ 2016C$
Low-side switch	E_2	$EPC\ 2001C$

Taking into account the discussions performed for Figure 2, two distinct PCB layouts are designed and represented in Figures 3 (a) and (b). These consider the converter electrical parameters presented in Table I. The width and length for tracks in layouts 1 and 2 are shown in Table II. PCB layer stack-ups are presented in Figures 4 (a) and (b). The main differences between the layouts are related to the number of copper planes (2 and 4), copper plane thickness ($1oz$ and $2oz$), PCB thickness ($1mm$ and $1.6mm$), number of vias and the PCB path area.

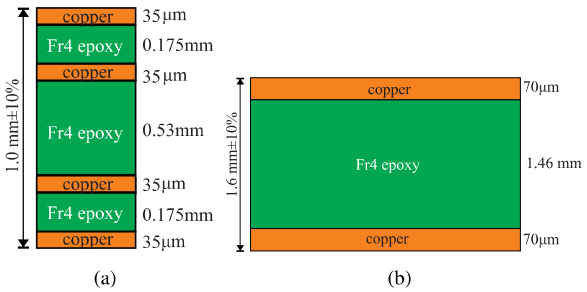


(a)



(b)

Fig. 3. Synchronous boost converter and its PCB paths distribution. (a) Layout 1 (b) Layout 2.



(a) (b)

Fig. 4. PCB layer stack-up. (a) Layout 1. (b) Layout 2.

Layouts 1 and 2 are used to create the 3-D thermal resistance network, relating their electrical and thermal characteristics. The model uses temperature-dependent electrical losses and a 3-D thermal resistance network to find the temperatures of the components. A flowchart that represents the steps in the

TABLE II
LENGTH AND WIDTH FOR PCB PATHS IN LAYOUT 1 AND 2.

Track	Layout 1 (mm) Length	Layout 1 (mm) Width	Layout 2 (mm) Length	Layout 2 (mm) Width
1	$l_1 = 19.93$	$w_1 = 8.0$	$l_1 = 34.60$	$w_1 = 7.5$
2	$l_2 = 10.48$	$w_2 = 7.54$	$l_2 = 11.33$	$w_2 = 9.03$
3	$l_3 = 2.5$	$w_3 = 6.32$	$l_3 = 4.0$	$w_3 = 34.6$
4	$l_4 = 3.0$	$w_4 = 33.60$	$l_4 = 21.19$	$w_4 = 21.92$

proposed method is shown in Figure 5, and its application in layouts 1 and 2 are explained in Sections III-A and III-B, respectively. The steps for Figure 5 are described as follows:

- Step 1: Input parameters definition, in which the PCB designer has to inform: the PCB layout mechanical characteristics; initial value of heat sources related to power losses in components, P_{E1}, P_{E2} and P_{E3}, which are, respectively, the inductor power losses, the low-side transistor and high-side transistor losses; ambient parameters; and the power converter electrical characteristics.
- Step 2: PCB paths conversion. Where the PCB paths are converted into thermal resistances and applied to a 3-D thermal resistance model. A mathematical software calculates all coefficients that influence the heat transfer process among the heat sources and the ambient. In the convection process, it is necessary to calculate R_a, Nu, and $R_{\theta conv}$. Moreover, $R_{\theta cond}$ is defined in every PCB path. $R_{\theta rad}$ is only calculated regarding the inductor surface. Also $R_{\theta PCB}$, $R_{\theta vias}$, η_a, $k_{bottom_{ind}}$ and all thermal parameters are applied to the model. As an example, Appendix A provides the equations for layout 1.
- Step 3: Linear system definition and solution, where the model defined in step 2 for each layout is solved using mathematical software.
- Step 4: Results acquisition. Where the superficial temperature estimation in the inductor (T_{E1}), low-side (T_{E2}) and high-side (T_{E3}) semiconductors, and the T_2 path (T_{T2}).
- Step 5: Power losses iteration. The power losses are recalculated, considering the temperatures calculated in Step 4 and their influence on drain-to-source on-state resistance (RDSon) (electro-thermal model).
- Step 6: Temperature actualization. Step 3 is repeated with the power losses calculated in Step 5.
- Step 7: Final step. This process is repeated until the temperature obtained in the steady state is lower than 1% related to the temperature obtained in the last update.

A. Thermal model - Layout 1

The thermal model for the synchronous boost converter layout 1 is composed of a 3-D thermal resistance network (Figure 6). The red cylinders represent the thermal resistance and the gray blocks are the heat sources (inductor and semiconductor switches). In all connections between two thermal resistances, it is possible to obtain an estimated temperature. However, the yellow pyramids highlight important points in the model. The specific location of the pyramids was chosen to estimate the main elements temperature (inductor and

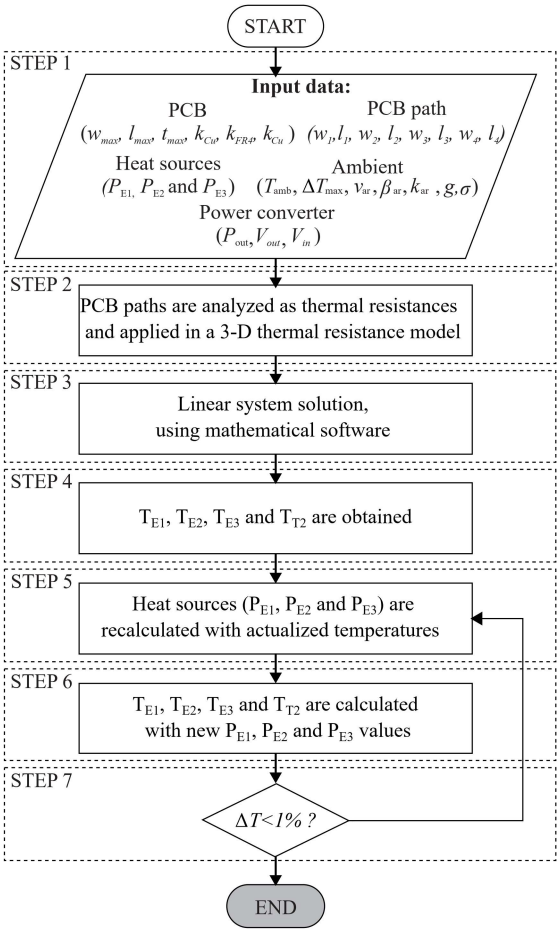


Fig. 5. Proposed analytical method flowchart.

switches) and the PCB path representing a thermal and electric connection link.

Also, toroids represent thermal vias and the blue dots are the T_∞ point (ambient temperature). It is assumed that the three heat sources (inductor, low-side switch, and high-side switch) dissipate heat through the x, y, and z axes. In each block, there will be convection at the central point both in the upward and downward directions after the heat passes through the FR4 layer of the PCB to the surroundings.

In T_1 PCB path the methodology assumes the heat transfer only occurs in the top/down and front/back direction (x and z axis). Although, the T_2 PCB path is wider than T_1, T_3, and T_4 because it connects the inductor and the semiconductor switches. The T_2 PCB path is a thermal interface between all the thermal sources of the system. Thus, it is considered that heat transfer occurs along the surface of T_2. The thermal resistances R_1 and R_2 represent the opposition to the heat transfer in the front/back direction (x-axis), and R_3 represent the thermal resistance in the left/right direction (y-axis). So, with this developed network of thermal resistances, it is possible to determine T_{T2} in a central point of T_2, where the designer can define its distances along the x and y axis or the distance of the main components.

To calculate the temperature in the inductor, semiconduc-

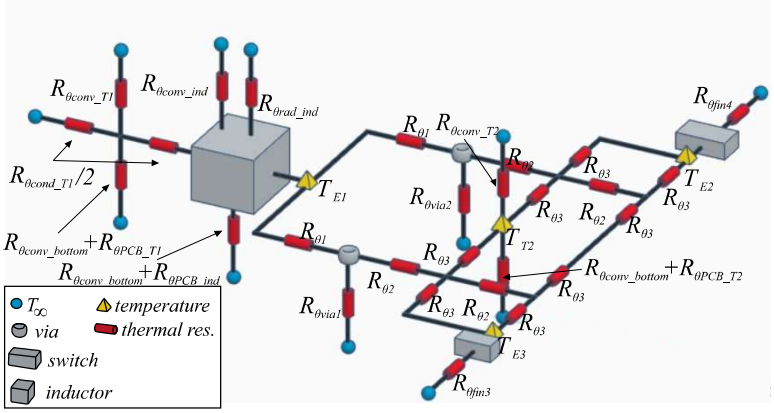


Fig. 6. 3-D thermal resistances network model developed.

$$
\begin{aligned}
T_{T1}.(2k_{cond}+k_{bottom}+k_{convT1}+2k_{cond})-T_{E1}.2k_{cond}-T_\infty.2k_{cond}-T_\infty.k_{bottom}-T_\infty.k_{convT1}=0\\
T_{E1}.(k_{eq}+k_{bottom_{ind}}+2k_{cond}+2k_{k_1})-T_{T1}.2k_{cond}-T_{p1}.k_1-T_{p3}.k_1=P_{E1}+T_\infty.k_{eq}+T_\infty.k_{bottom_{ind}}+T_\infty\\
T_{p1}.(k_1+k_2+k_3+k_{via1})-T_{E1}.k_1-T_{E2}.k_3-T_{p6}.k_2-T_\infty.k_{via1}=0\\
T_{p2}.(k_2+k_3+\tfrac{k_3}{2})-T_{p4}.\tfrac{k_3}{2}-T_{E2}.k_3-T_{p6}.k_2=0\\
T_{p3}.(k_1+k_2+k_3+k_{via2})-T_{p1}.k_1-T_{p7}.k_2-T_{E3}.k_3-T_\infty.k_{via2}=0\\
T_{p4}.(k_2+k_3+\tfrac{k_3}{2})-T_{p2}.\tfrac{k_3}{2}-T_{p7}.k_2-T_{E3}.k_3=0\\
T_{T2}.(k_3+k_3+k_{convT2}+k_{bottom})-T_{p6}.k_3-T_{p7}.k_3=T_\infty.k_{convT2}+T_\infty.k_{bottom}\\
T_{p6}.(2.k_2+k_3)-T_{p1}.k_2-T_{p2}.k_2-T_{T2}.k_3=0\\
T_{p7}.(2.k_2+k_3)-T_{p3}.k_2-T_{p4}.k_2-T_{T2}.k_3=0\\
T_{E2}=P_{E2}.\eta_{a4}.k_{fin_4}+T_\infty\\
T_{E3}=P_{E3}.\eta_{a3}.k_{fin_3}+T_\infty
\end{aligned}
\tag{13}
$$

tors, and PCB paths on the PCB layout, a linear system is expressed in (13), using the thermal conductance as the inverse of thermal resistances presented in Section II. The term R_{condT1} is defined with equation (1); the term $R_{\theta PCBind}$ is calculated appliying the equation (2); R_{convT1} is calculated through (7), (8), (9), (10); $R_{\theta radind}$ is defined with (11); $R_{\theta via1}$ through (3), (5), (4) and (6); $R_{\theta fin3}$ is defined through (12).

Information for all the coefficients presented in Figure 6 are in Appendix A. Using these coefficients, the length and width for PCB paths presented in Table II, areas related to SMD inductor and transistors, as well as the PCB dimensions presented in Figure 3 (a); the thermal resistances are calculated and presented in Table III.

The core losses in the inductor (P_{E1}), are estimated using the Improved Generalized Steinmetz Equation (IGSE) and Natural Steinmetz Equation (NSE), presented in [34], [35], which take into account the triangular characteristic of the current waveform circulating through the inductor. Copper losses and temperature are defined as [34].

To calculate the losses in high-side and low-side switches (P_{E2} and P_{E3}), the models presented in [36], [37] are used. First, the conduction, switching, and reverse recovery losses are calculated for the ambient temperature. This is used in (13) to find the temperature in the component. After, losses are recalculated, considering the new temperature and its influence in drain-to-source on-state resistance (R_{DSon}) (electro-thermal model).

TABLE III
THERMAL RESISTANCES CALCULATED FOR LAYOUT 1.

Parameter	Thermal resistance $°C\ /W$
$R_{\theta cond1}$	128
$R_{\theta conv1}$	340
$R_{\theta conv\_bottom}+R_{\theta PCB1}$	164.18
$R_{\theta conv\_ind}$	50.98
$R_{\theta rad\_ind}$	89.23
$R_{\theta conv\_bottom}+R_{\theta PCBind}$	160.46
$R_{\theta 1}$	50
$R_{\theta 2}$	31
$R_{\theta 3}$	71.27
$R_{\theta conv\_bottom}+R_{\theta PCB\_T2}$	175.51
$R_{\theta conv\_T2}$	530
$R_{\theta fin3}$	472.554
$R_{\theta fin4}$	411.756
$R_{\theta via1}$	185.631

The behavior of the $R_{DSon} \times T_J$ is provided by the manufacturer and is represented as,

$$R_{DSon(T_J)} = R_{DSon(25°C)}.\left(1+\frac{\alpha}{100}\right)^{T_J-25°C} \tag{14}$$

where T_J is the junction temperature, $R_{DSon(25°C)}$ is the value of R_{DSon} at 25 °C, and α is the temperature coefficient, obtained from the slope of the $R_{DSon} \times T_J$. The on-state (conduction) losses P_C can be calculated as,

$$P_C = R_{DSon(Tj)}{I_{RMS}}^2. \tag{15}$$

Analytical results found for 50 W and 75 W in layout 1 are presented in Table IV, including power losses and the main temperature points in the power converter.

TABLE IV
ANALYTICAL RESULTS ACQUIRED IN LAYOUT 1.

Parameter	$P_{out} = 50W$	$P_{out} = 75W$
P_{E1}	$1.1W$	$2W$
P_{E2}	$0.84W$	$1.4W$
P_{E3}	$0.3W$	$0.65W$
T_{E1}	$59.58°C$	$92.68°C$
T_{E2}	$78.74°C$	$122.56°C$
T_{E3}	$67.70°C$	$112.57°C$
T_{T2}	$59.87°C$	$92.68°C$

B. Thermal model - Layout 2

In layout 2, the superficial area is increased by 62.71% when compared with layout 1, and PCB layers are reduced from four to two, as presented in Figure 4 (b). This results in the PCB copper plane thickness (t_{cu}) being two times higher related to layout 1. Heat conduction and convection, as well as thermal paths and their equivalent resistance, are calculated according to Section II. The 3-D thermal model of thermal resistances representing layout 2 is shown in Figure 7.

It is assumed that the three heat sources (inductor, low-side switch, and high-side switch) dissipate heat through the x, y, and z axes, where tracks T_3 and T_4 is now divided into three small blocks with specific length, width, and area. In each block, there will be convection at the central point both in the upward and downward directions after the heat passes

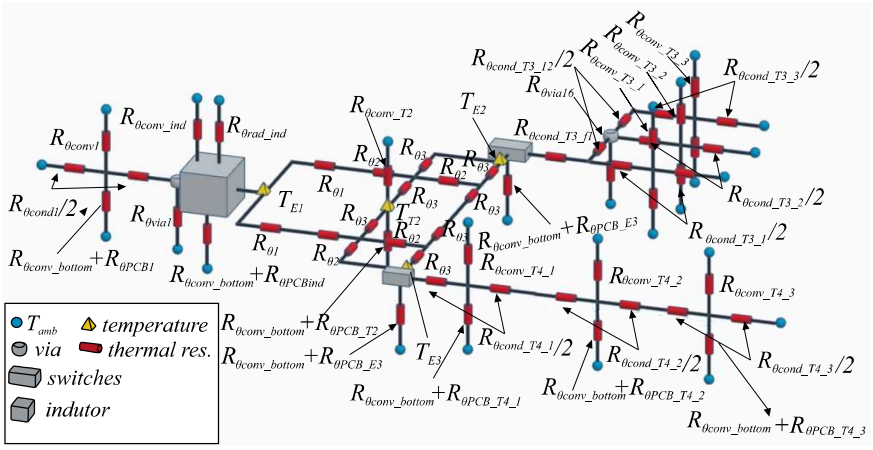


Fig. 7. 3-D thermal resistances network model developed for layout 2.

$$
\begin{gathered}
T_{T1}.(2k_{cond} + k_{bottom} + k_{convT1} + 2k_{cond}) - T_{E1}.2k_{cond} - T_{\infty}.2k_{cond} - T_{\infty}.k_{bottom} - T_{\infty}.k_{convT1} = 0 \\
T_{E1}.(k_{eq} + k_{bottomind} + 2k_{cond} + 2k_{k_1} + k_{via1}) - T_{T1}.2k_{cond} - T_{p1}.k_1 - T_{p3}.k_1 = P_{E1} + T_{\infty}.k_{eq} + T_{\infty}.k_{bottomind} + T_{\infty}.k_{via1} \\
T_{p1}.(k_1 + k_2 + k_3) - T_{E1}.k_1 - T_{E2}.k_3 - T_p6.k_2 = 0 \\
T_{p2}.(k_2 + k_3 + \tfrac{k_3}{2}) - T_{p4}.\tfrac{k_3}{2} - T_{E2}.k_3 - T_{p6}.k_2 = 0 \\
T_{p3}.(k_1 + k_2 + k_3) - T_{p1}.k_1 - T_{p7}.k_2 - T_{E3}.k_3 = 0 \\
T_{p4}.(k_2 + k_3 + \tfrac{k_3}{2}) - T_{p2}.\tfrac{k_3}{2} - T_{p7}.k_2 - T_{E3}.k_3 = 0 \\
T_{T2}.(k_3 + k_3 + k_{convtop} + k_{bottom}) - T_{p6}.k_3 - T_{p7}.k_3 = T_{\infty}.k_{convtop} + T_{\infty}.k_{bottom} \\
T_{p6}.(2.k_2 + k_3) - T_{p1}.k_2 - T_{p2}.k_2 - T_{T2}.k_3 = 0 \\
T_{p7}.(2.k_2 + k_3) - T_{p3}.k_2 - T_{p4}.k_2 - T_{T2}.k_3 = 0 \\
T_{E2}.(2k_3 + k_{bottome2} + k_{condT3f1}) - T_{p1}.k_3 - T_{p2}.k_3 - Tp311.k_{condT3f1} = P_{E2} + T_{\infty}.k_{bottome2} \\
T_{p311}.(k_{condT3f1} + 2k_{condT312} + k_{condT31}) - T_{E3}.k_{condT3f1} - T_{p322}.(k_{condT312} - T_{T31}.k_{condT31} = 0 \\
T_{T31}.(k_{convT31} + k_{convbottomT31} + 4k_{condT31}) - T_{p311}.2k_{condT31} = T_{\infty}.k_{convT31} + T_{\infty}.k_{convbottomT31} \\
T_{p322}.(4k_{condT312} + 2k_{condT32} + k_{via16}) - T_{p311}.(2k_{condT312} - T_{p33}.2k_{condT312} = T_{\infty}.k_{via16} \\
T_{T32}.(k_{convT32} + k_{convbottomT32} + 4k_{condT32}) - T_{p322}.2k_{condT32} = T_{\infty}.k_{convT32} + T_{\infty}.k_{convbottomT32} \\
T_{p33}.(2k_{condT312} + 2k_{condT33}) - T_{p322}.(2k_{condT312} - T_{T33}.2k_{condT33} = 0 \\
T_{T33}.(k_{convT33} + k_{convbottomT33} + 4k_{condT33}) - T_{p333}.2k_{condT33} = T_{\infty}.k_{convT33} + T_{\infty}.k_{convbottomT33} \\
T_{E3}.(2k_3 + k_{bottome3} + 2k_{condT41}) - T_{p3}.k_3 - T_{p4}.k_3 - T_{T41}.2k_{condT41} = P_{E3} + T_{\infty}.k_{bottome3} \\
T_{T41}.(k_{convT41} + k_{convbottomT41} + 4k_{condT41}) - T_{E3}.2k_{condT41} - T_{p412}2k_{condT41} = T_{\infty}.k_{convT41} + T_{\infty}.k_{convbottomT41} \\
T_{p412}.(2k_{condT41} + 2k_{condT42}) - T_{T41}.2k_{condT41} - T_{T42}.2k_{condT42} = 0 \\
T_{T42}.(k_{convT42} + k_{convbottomT42} + 4k_{condT42}) - T_{p412}.2k_{condT42} - T_{p423}2k_{condT42} = T_{\infty}.k_{convT42} + T_{\infty}.k_{convbottomT42} \\
T_{p423}.(2k_{condT42} + 2k_{condT43}) - T_{T42}.2k_{condT42} - T_{T43}.2k_{condT43} = 0 \\
T_{T43}.(k_{convT43} + k_{convbottomT43} + 4k_{condT43}) - T_{p423}.2k_{condT43} = T_{\infty}.k_{convT43} + T_{\infty}.k_{convbottomT43} + T_{\infty}.2k_{condT43}
\end{gathered}
\tag{16}
$$

through the FR4 layer of the PCB to the surroundings. The linear system that relates different temperatures along the 3D thermal resistance model is given in equation (16), where the main points of interest are T_{E1}, T_{E2}, T_{E3}, and T_{T2}.

Considering the dimensions presented in Table II, the areas corresponding to the inductor and semiconductor switches, as well as the physical dimensions of the PCB shown in Figure 3 (b), the calculated values for the analytical method of layout 2 can be verified in Table V. The coefficients presented in Figure 7 can be found in the same way as for layout 1.

TABLE V
THERMAL RESISTANCES CALCULATED FOR LAYOUT 2.

Parameter	Thermal resistance $°C\ /W$
$R_{\theta cond1}$	41.48
$R_{\theta conv1}$	276
$R_{\theta conv\_bottom} + R_{\theta PCB1}$	82.79
$R_{\theta conv\_ind}$	50.98
$R_{\theta rad\_ind}$	89.23
$R_{\theta conv\_bottom} + R_{\theta PCBind}$	82.86
$R_{\theta via1}$	61.87
$R_{\theta 1}$	99.11
$R_{\theta 2}$	70.27
$R_{\theta 31}$	52.09
$R_{\theta conv\_bottom} + R_{\theta PCB\_T2}$	93.25
$R_{\theta conv\_T2}$	504
$R_{\theta conv\_bottom} + R_{\theta PCB\_E2}$	574.91
$R_{\theta conv\_bottom} + R_{\theta PCB\_T3\_1}$	128.25
$R_{\theta cond\_T3\_f1}$	168.46
$R_{\theta cond\_T3\_1}$	126.52
$R_{\theta conv\_T3\_1}$	956.87
$R_{\theta conv\_T3\_12}$	166.25
$R_{\theta conv\_bottom} + R_{\theta PCB\_T3\_2}$	97.96
$R_{\theta cond\_T3\_2}$	263.82
$R_{\theta conv\_T4\_2}$	1431
$R_{\theta via16}$	11.6
$R_{\theta conv\_bottom} + R_{\theta PCB\_T4\_3}$	128.25
$R_{\theta cond\_T4\_3}$	448.05
$R_{\theta conv\_T4\_3}$	956.87
$R_{\theta conv\_bottom} + R_{\theta PCB\_E3}$	956.53
$R_{\theta conv\_bottom} + R_{\theta PCB\_T4\_1}$	100.71
$R_{\theta cond\_T4\_1}$	164.26
$R_{\theta conv\_T4\_1}$	674.77
$R_{\theta conv\_bottom} + R_{\theta PCB\_T4\_2}$	289.08
$R_{\theta cond\_T4\_2}$	160.44
$R_{\theta conv\_T4\_2}$	1431
$R_{\theta conv\_bottom} + R_{\theta PCB\_T4\_3}$	147.30
$R_{\theta cond\_T4\_3}$	132.52
$R_{\theta conv\_T4\_3}$	1430

Analytical results found for 50 W and 75 W in layout 2 are presented in Table VI, including power losses and the main temperature points in the power converter.

TABLE VI
ANALYTICAL RESULTS ACQUIRED IN LAYOUT 2.

Parameter	$P_{out} = 50W$	$P_{out} = 75W$
P_{E1}	$1.122W$	$1.9W$
P_{E2}	$0.84W$	$1.25W$
P_{E3}	$0.4W$	$0.65W$
T_{E1}	$57.01°C$	$80.01°C$
T_{E2}	$79.55°C$	$112.86°C$
T_{E3}	$68.81°C$	$97.86°C$
T_{T2}	$60.58°C$	$84.19°C$

IV. FEA AND EXPERIMENTAL SETUP DESCRIPTION

The proposed analytical method is validated through measurements on experimental prototypes and from the FEA in Layout 1 and Layout 2. In the experimental approach, to account for variations in emissivity (ε) values of the components within the boost converter, a layer of matte black paint (standardizing ε to 0.95) is applied to the surface of the two prototypes under analysis. This is illustrated in Figure 8 (a) and (b) for layouts 1 and 2 respectively. To enhance the accuracy of thermal measurements, the use of a heat sink and forced ventilation are not used. This decision is made considering that the thermal resistance of a heat sink is nonlinear concerning factors such as length, number of fins, air flux, and altitude, among others [21], [36], [38], [39].

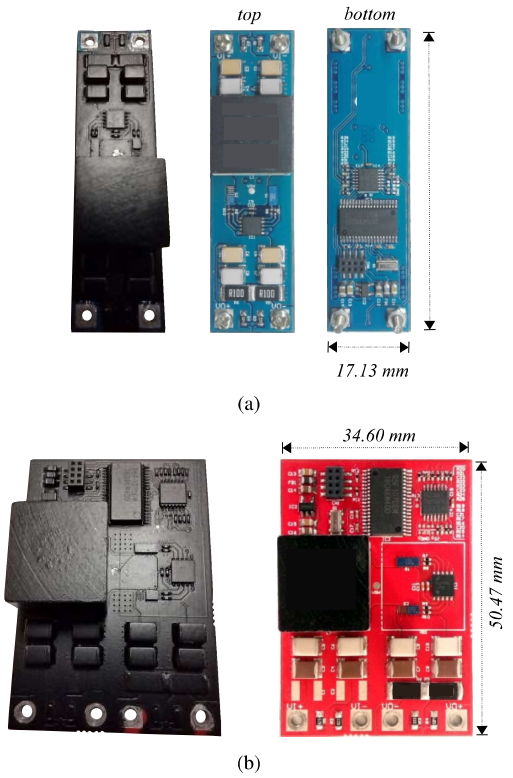


Fig. 8. Power converter prototype painted with matte black paint. (a) Layout 1. (b) Layout 2.

The test bench and the support box for the prototypes under test are depicted in Figure 9. Temperature measurements are conducted using a high-sensitivity thermal camera ($\pm 2°C$, FLIR A6753sc). Monitoring of current, voltage, and power in the circuit is performed by an oscilloscope and a power meter. The circuit is powered by a DC voltage source, and two LEDs with a maximum power of 100 W are employed as the loads.

In addition, an FEA is developed using Ansys ICEPAK to estimate junction and case temperatures of semiconductor switches, as well as the internal and top temperatures of the inductor. This allows for a comparison between measurements and the proposed analytical method. The construction of the model for both configurations necessitates a comprehensive

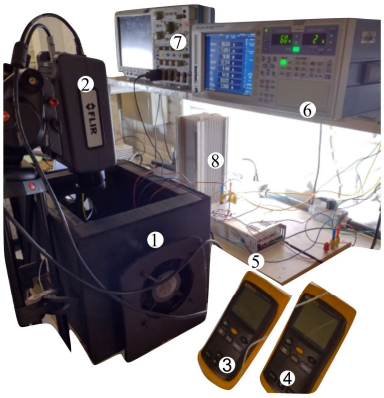


Fig. 9. Test bench.

incorporation of key elements. This includes the 3D design, physical dimensions, and thermal conductivity properties of the copper winding materials within the inductor and its core. Additionally, careful consideration must be given to the semiconductor switch elements, encompassing the solder points connecting these components to the printed circuit board (PCB).

The assessment also includes the evaluation of airflow velocity in the x, y, and z directions, as well as mesh refinement properties. The materials and their thermal characteristics specified in the developed model are presented in Table VII.

TABLE VII
THERMAL CONDUCTIVITY OF THE MATERIALS USED IN THE FEA MODEL DEVELOPED IN THE ANSYS ICEPAK *software*

Element	**Material**	**Thermal conductivity** $(W/m°C)$
High-side switch	Silicon	148
Low-side switch	Silicon	148
Solder	$Pb50\_Sn50$	46
Inductor turns	copper	400
Inductor core	$AZ91_{MMC}$	38.7
Inductor package	$AZ91$	60.5
PCB paths	copper	400
PCB region	air ($20°C$)	0.0261
PCB dielectric	FR4 epoxy	0.294
DUT support box	wood	0.113

For an accurate FEA simulation, the computational environment replicates the same dimensions of a wooden box with an upper opening and lateral vents. The ambient temperature is set to $20°C$. Furthermore, heat generation points are defined as the copper winding of the inductor and the central points of the silicon cubes designated as the high-side and low-side switches.

Through the convergence of the simulation, results are obtained for different temperatures across the analyzed PCB, air displacement vectors and air heating near the heat sources due to convection and radiation processes.

The boundary conditions of the model developed in Ansys Icepak software include an ambient temperature of $20°C$, the presence of gravitational force, turbulent flow, and a surrounding region around the PCB extending 500% in all directions. Additionally, an estimated low wind speed in the x-direction, $v_x = 0.13m/s$, is considered due to the lateral openings in the DUT support box. Furthermore, the semiconductor switches, with power losses P_{E2} and P_{E3} located within a silicon block, and the copper winding of the inductor, with power losses P_{E1}, are designated as the 'thermal box' elements.

V. EXPERIMENTAL THERMAL VALIDATION

As aforementioned, the FEA analysis of the PCB layout is conducted using Ansys Icepak. The external region is modeled based on the laboratory test bench, as shown in Figure 9. The ambient temperature is controlled at $T_\infty = 20°C$, and the air within the region is influenced by gravity force. Losses are considered as presented in Section III.

Considering the power converter with layout 1, Figures 10 (a) and (b) present the temperature distribution along the PCB top layer for $P_{out} = 50W$ and $P_{out} = 75W$, respectively. It is crucial to note that the FEA is conducted on a workstation with an 18-core, $2.3GHz$ processor, $64GB$ RAM, a graphics card with 640 GPU cores, and $4GBDDR5$ memory. The FEA analysis for the PCB layout took approximately ten hours to compute the results.

The thermal results of the power converter in the experimental prototype, considering layout 1, are depicted in Figures 11 (a) and (b) for $P_{out} = 50W$ and $P_{out} = 75W$, respectively. In both conditions, the low-side switch exhibits the highest temperature along the top of the PCB, followed by the high-side switch and inductor. The low-side switch exhibits higher losses than the high-side due to the power converter gain, which is about 4.5, consequently presenting the higher temperature.

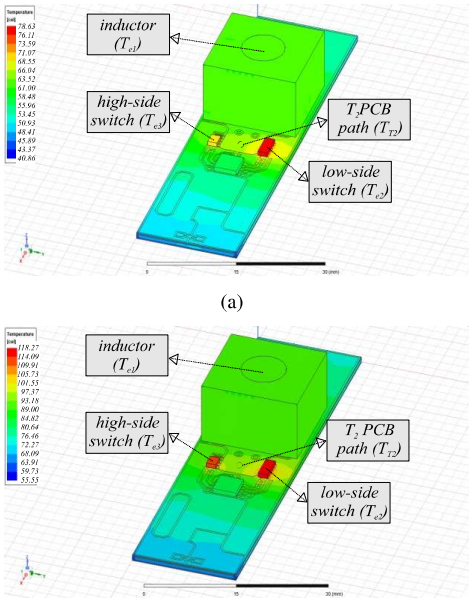


Fig. 10. Temperature distribution in the top layer of the PCB acquired with FEA. (a) $P_{out} = 50W$, $P_{E1} = 1.1W$, $P_{E2} = 0.84W$, $P_{E3} = 0.3W$. (b) $P_{out} = 75W$, $P_{E1} = 2W$, $P_{E2} = 1.4W$, $P_{E3} = 0.65W$.

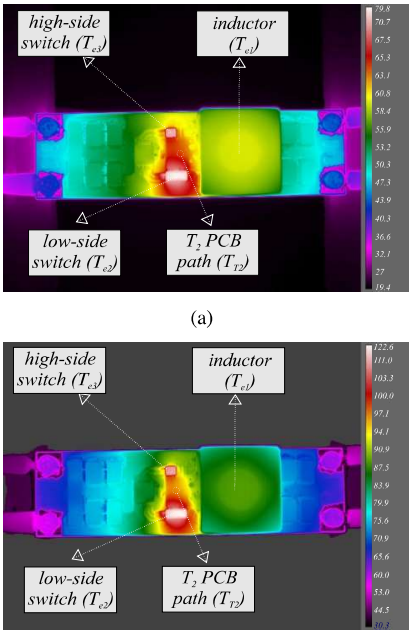


Fig. 11. Experimental thermal measurements for synchronous boost converter, $13mm$ lens, $10cm$ from object, $\varepsilon = 0.95$. (a) $P_{out} = 50W$. (b) $P_{out} = 75W$, scale from $30°C$ to $150°C$.

The temperatures obtained for layout 1 using the proposed analytical method are compared with measurements and FEA in Table VIII for 50W, and in Table IX for 75W. The error column evaluates the error between the proposed analytical method and the prototype measurement.

TABLE VIII
THERMAL RESULTS ACQUIRED WITH $P_{out} = 50W$.

Parameter	Proposed	FEA	Prototype	Error
T_{E1}	$59.58°C$	$62.46°C$	$57.8°C$	3.08%
T_{E2}	$78.74°C$	$78.63°C$	$78.9°C$	0.2%
T_{E3}	$67.70°C$	$70.61°C$	$70.5°C$	3.97%
T_{T2}	$59.87°C$	$56.68°C$	$63.7°C$	6.01%

TABLE IX
THERMAL RESULTS ACQUIRED WITH $P_{out} = 75W$.

Parameter	Proposed	FEA	Prototype	Error
T_{E1}	$92.68°C$	$90.31°C$	$85.0°C$	9.03%
T_{E2}	$122.56°C$	$118.27°C$	$120.6°C$	1.62%
T_{E3}	$112.57°C$	$110.16°C$	$109.5°C$	2.80%
T_{T2}	$93.24°C$	$97.11°C$	$94.7°C$	1.54%

As presented in Table VIII and Table IX, the T_{T2} and T_{E1} have shown the highest source of error, respectively. The T_2 PCB path is an interface among three thermal sources (P_{E1}, P_{E2} e P_{E3}), so the three sources of errors can impact the T_{T2} estimation. Also, T_{E1} can be impacted by the thermal losses estimated in the inductor and the errors in the estimated T_{E2} and T_{E3}. In layout 1, the average error for 50 W and 75 W are 3.74% and 3.31%, respectively.

For the power converter with layouts 2, Figures 12 (a) and (b) present the temperature distribution along the PCB top layer for $P_{out} = 50W$ and $P_{out} = 75W$, respectively. The thermal results of the power converter in the experimental prototype, considering layout 2, are depicted in Figures 13 (a) and (b) for $P_{out} = 50W$ and $P_{out} = 75W$, respectively. As for layout 1, in both conditions, the low-side switch exhibits the highest temperature along the top of the PCB, followed by the high-side switch and the inductor.

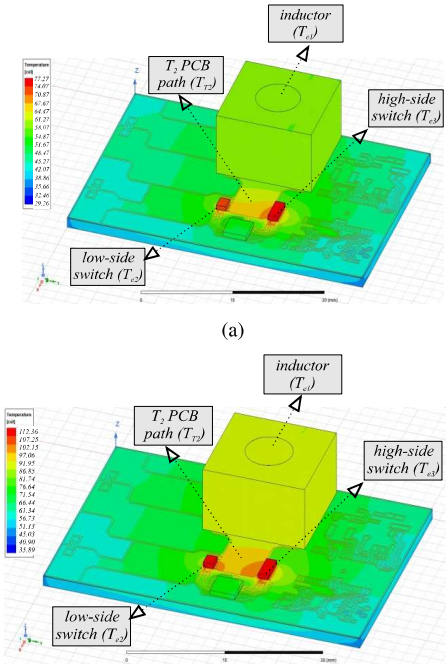


Fig. 12. Temperature distribution in the top layer of the PCB acquired with FEA. (a) $P_{out} = 50W$, $P_{E1} = 1.122W$, $P_{E2} = 0.84W$, $P_{E3} = 0.4W$. (b) $P_{out} = 75W$, $P_{E1} = 1.9W$, $P_{E2} = 1.25W$, $P_{E3} = 0.65W$.

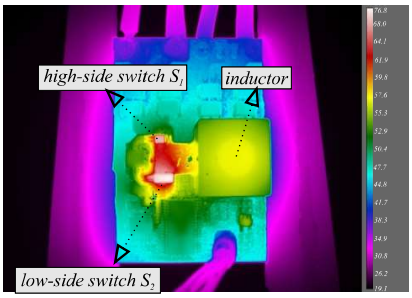
The temperatures obtained for layout 2 using the proposed analytical method are compared with measurements and FEA in Table X for 50W, and in Table XI for 75W. The T_{E2} and T_{E3} have presented the highest source of error in the layout 2 thermal model. Thus, T_{E2} can be impacted by the proximity of the auxiliary components in the PCB (gate driver, microcontroller) and the irregularity of T_3 PCB path. Also, T_{E3} could be impacted by the error in the power loss estimation and the irregularity in the T_4 PCB path. In layout 2, the average error for 50 W and 75 W are 2.69% and 2.64%, respectively.

TABLE X
THERMAL RESULTS ACQUIRED WITH $P_{out} = 50W$.

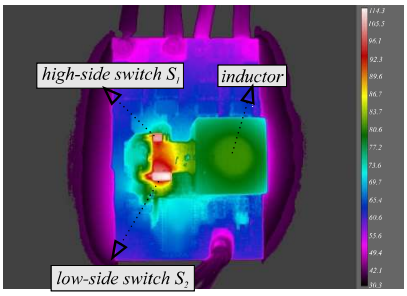
Parameter	Proposed	FEA	Prototype	Error
T_{E1}	$57.01°C$	$61.46°C$	$55.5°C$	2.72%
T_{E2}	$79.55°C$	$77.27°C$	$76.2°C$	4.39%
T_{E3}	$68.81°C$	$73.50°C$	$67.9°C$	1.34%
T_{T2}	$60.58°C$	$63.90°C$	$61.9°C$	2.13%

TABLE XI
THERMAL RESULTS ACQUIRED WITH $P_{out} = 50W$.

Parameter	Proposed	FEA	Prototype	Error
T_{E1}	$80.01°C$	$90.36°C$	$77.3°C$	3.51%
T_{E2}	$112.86°C$	$112.36°C$	$112.3°C$	0.5%
T_{E3}	$97.86°C$	$108.85°C$	$101.6°C$	3.68%
T_{T2}	$84.19°C$	$94.56°C$	$86.7°C$	2.89%



(a)



(b)

Fig. 13. Experimental thermal measurements for synchronous boost converter, $13mm$ lens, $10cm$ from object, $\varepsilon = 0.95$. (a) $P_{out} = 50W$. (b) $P_{out} = 75W$, scale from $30°C$ to $150°C$.

VI. CONCLUSIONS

This work presented an accurate analytical electro-thermal model and a 3-D thermal resistance network for an SMD-based synchronous commutation cell. These are used to estimate temperature distribution for a synchronous boost converter. Additionally, the method can be used in every power converter based on a synchronous commutation cell.

The results obtained by the proposed analytical method are compared to prototype measurements and FEA with two different layouts and two different loads. Results found for both layout 1 and layout 2 demonstrated good accuracy, with average temperature errors related to prototype measurements of 3.74% and 2.69%, respectively. Furthermore, only a specific point of analysis showed an error exceeding 9% compared to the experimental prototype, thus validating the effectiveness of the proposed methodology.

As the analytical method is based on equations, it is significantly faster compared to the numerical method developed through FEA analysis. This enables the PCB designer to evaluate various layouts of their project within seconds rather than spending several hours with FEA analysis. The analytical method also can be used by the PCB designer to test and compare different scenarios before the prototyping process, such as different PCB path mechanical characteristics and the thermal interaction among the elements and the ambient.

APPENDIX

3-D thermal resistances network model and equation (13) coefficients calculation:

$$k_{cond} = \frac{1}{R_{cond1}} = \frac{1}{\frac{l_1}{k_{Cu}.t_{Cu}.w_1}} \tag{17}$$

where l_1 and w_1 are the T_1 length and width;

$$k_{bottom} = \frac{1}{\frac{L_{Cbottom}}{k_{air}.Nu_{bottom}.A_{bottom}}} \tag{18}$$

where A_{bottom} is the bottom area of the PCB, Nu_{bottom} the Nusselt coefficient from the bottom of the PCB.

$$k_{convT1} = \frac{1}{\frac{L_{CT1}}{k_{air}.Nu_{T1}.A_{T1}}} \tag{19}$$

where

$$k_{eq} = \frac{1}{R_{conv_{ind}} + R_{rad_{ind}}} \tag{20}$$

where $R_{conv_{ind}}$ and $R_{rad_{ind}}$ are the convection and radiation thermal resistances from the inductor.

$$k_1 = \frac{1}{\frac{l_2}{w_2.t_{Cu}.k_{Cu}} - \frac{1}{k_2}} \tag{21}$$

where l_2 and w_2 are the T_2 length and width.

$$k_2 = \frac{1}{\frac{0.0055}{w_2.t_{Cu}.k_{Cu}}} \tag{22}$$

$$k_3 = \frac{1}{\frac{w_2}{l_2.t_{Cu}.k_{Cu}}} \tag{23}$$

$$k_{bottom_{ind}} = \frac{1}{\frac{t-2.t_{Cu}}{k_{FR4}.A_{ind}} + k_{bottom}} \tag{24}$$

where t is the PCB thickness.

$$k_{via1} = k_{via2} = \frac{1}{\frac{R_{\theta filler}.R_{\theta barrel}}{R_{\theta filler}+R_{\theta barrel}}} \tag{25}$$

$$k_{convT2} = \frac{1}{\frac{L_{C2}}{k_{air}.Nu_2.A_2}} \tag{26}$$

$$\eta a_3 = \frac{tanh(m_3.L_{C3})}{m_3.L_{c3}} \tag{27}$$

where L_{C3} is the fin critical length.

$$m_3 = \sqrt{\frac{h_3.p_3}{k_{Cu}A_3}} \tag{28}$$

where h_3 is the convection coefficient, A_3 the fin area, p_3 the fin perimeter.

$$\eta a_4 = \frac{tanh(m_4.L_{C4})}{m_4.L_{C4}} \tag{29}$$

$$k_{fin3} = \frac{1}{\eta a_3.h_3.L_3.w_3} \tag{30}$$

where ηa_3 is the fin efficiency, h_3 the convection coefficient, L_3 and w_3 the fin length and width;

$$k_{fin4} = \frac{1}{\eta a_4.h_4.L_4.w_4} \tag{31}$$

$$q_{te2} = P_{E2}.\eta a_3 \tag{32}$$

where P_{E2} is the power loss from the low-side semiconductor switch;

$$q_{te3} = P_{E3}.\eta a_4 \tag{33}$$

where P_{E3} is the power loss from the low-side semiconductor switch.

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